IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A process of treating a semiconductor structure comprising:

providing a substrate;

providing a gate stack comprising a gate dielectric layer disposed over the substrate; a polysilicon layer disposed over the gate dielectric layer; a barrier layer disposed over the polysilicon layer, and a metal film disposed over the barrier layer;

patterning the metal film, barrier layer and polysilicon layer to form a pattered gate stack; and

oxidizing the patterned gate stack under conditions providing at least one of a halogen and a material having a thermodynamic advantage over the substrate in volatilizing the metal film that reduce redeposition of the metal film on the substrate and on the gate stack of a volatilized portion of the metal film.

2-4. (Canceled)

5. (Currently Amended) ~~The process according to claim 1,~~ A process of treating a semiconductor structure comprising:

providing a substrate;

providing a gate stack comprising a gate dielectric layer disposed over the substrate; a polysilicon layer disposed over the gate dielectric layer; a barrier layer disposed over the polysilicon layer, and a metal film disposed over the barrier layer;

patterning the metal film, barrier layer and polysilicon layer to form a pattered gate stack; and

oxidizing the patterned gate stack under conditions providing at least one of a halogen and a material having a thermodynamic advantage over the substrate in volatilizing the metal film that reduce redeposition of the metal film on the substrate and on the gate stack of a volatilized portion of the metal film;

wherein the conditions that reduce redeposition include using a fluorine-containing composition that is metered to the substrate and gate stack in gaseous form.

6. (Currently Amended) The process according to claim 5 [[1]], wherein the ~~conditions that reduce redeposition include using~~ fluorine-containing composition includes NF_3 gas ~~that is metered to the substrate and gate stack~~.

7. (Previously Presented) A process of treating a semiconductor structure comprising:

providing a substrate;

providing a gate stack comprising a gate dielectric layer disposed over the substrate; a polysilicon layer disposed over the gate dielectric layer; a barrier layer disposed over the polysilicon layer, and a metal film disposed over the barrier layer;

patterning the metal film, barrier layer and polysilicon layer to form a pattered gate stack; and

oxidizing the patterned gate stack under conditions providing at least one of a halogen and a material having a thermodynamic advantage over the substrate in volatilizing the metal film that reduce redeposition of the metal film on the substrate and on the gate stack of a volatilized portion of the metal film;

wherein the conditions that reduce redeposition include using a fluorine-containing composition disposed in a layer in the gate stack, and a fluorine-containing composition that is metered to the substrate and gate stack in gaseous form.

8. (Canceled)

9. (Original) A process comprising:

forming a metal film over a structure; and

thermally processing the structure in the presence of a first composition such that the metal is more likely to combine with at least a portion of the first composition than with the structure.

10. (Original) The process according to claim 9, wherein the structure comprises oxide surfaces, and wherein the conditions are sufficient to cause the first composition to resist etching the oxide surfaces.

11. (Currently Amended) ~~The process according to claim 9,~~ A process comprising:

forming a metal film over a structure; and

thermally processing the structure in the presence of a first composition such that the metal is more likely to combine with at least a portion of the first composition than with the structure;

wherein the first composition comprises NF_3.

12. (Currently Amended) The process according to claim 11 [[9]], wherein the first composition comprises NF_3 in a gaseous state.

13. (Canceled)

14. (Original) The process according to claim 9, wherein the first composition comprises a halogen-containing composition.

15. (Original) The process according to claim 9, wherein the first composition comprises a halogen-containing composition in a gaseous state.

16. (Canceled)

17. (Previously Presented) The process according to claim 9, further comprising:

forming a spacer layer over the structure; and

etching the spacer layer.

18. (Previously Presented) A process comprising:

forming a doped polysilicon layer over a substrate;

forming a barrier layer over the doped polysilicon layer;

forming a metal film over the barrier layer;

forming a nitride layer over the metal film to form a gate stack disposed on a substrate; and

thermally processing the gate stack in the presence of a fluorine-containing composition under conditions sufficient to cause the metal film more likely to combine with the fluorine-containing composition than with the gate stack or the substrate.

19. (Original) The process according to claim 18, wherein the barrier layer includes a metal nitride barrier layer.

20. (Original) The process according to claim 18, wherein the gate stack and the substrate include oxide surfaces, and wherein the conditions are sufficient to cause the fluorine-containing composition to resist etching the oxide surfaces.

21. (Original) The process according to claim 18, wherein the fluorine-containing composition comprises NF_3.

22. (Original) The process according to claim 18, wherein the metal film is selected from Al, Cu, Ag, Au, Ti, Zr, Hf, Ni, Co, Pd, Pt, V, Ta, Nb, Cr, Mo, W, Sc, Yt, La, Ce, Rh, Os, Ir, and combinations thereof.

23-29. (Canceled)

30. (Previously Presented) A process of forming a gate stack comprising:

providing a substrate;

forming a gate dielectric layer over the substrate;

depositing a polysilicon layer over the gate dielectric layer;

forming a metal film above the polysilicon layer;

forming a cap layer over metal film;

etching a gate stack through the cap layer, the metal film, and the polysilicon layer, under conditions that reduce redeposition on the substrate of a volatilized portion of the metal film; and

wherein at least one process of depositing a polysilicon layer, forming a metal film, and forming a cap layer is carried out in the presence of a metal-reducing composition; and

oxidizing the polysilicon layer under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film.

31. (Previously Presented) The process according to claim 30 following etching a gate stack, further comprising:

forming a spacer layer over the gate stack under conditions providing at least one of a halogen and a material having a thermodynamic advantage over the substrate in volatilizing the metal film that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film.

32. (Previously Presented) A process of forming a gate stack comprising:

providing a substrate;

forming a gate dielectric layer over the substrate;

depositing a polysilicon layer over the gate dielectric layer;

forming a metal film above the polysilicon layer;

forming a cap layer over metal film;

etching a gate stack through the cap layer, the metal film, and the polysilicon layer, under conditions that reduce redeposition on the substrate of a volatilized portion of the metal film;

wherein at least one process of depositing a polysilicon layer, forming a metal film, and forming a cap layer is carried out in the presence of a metal-reducing composition;
following etching a gate stack, further comprising:

oxidizing the polysilicon layer under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film;

forming a spacer layer over the gate stack under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film; and

wherein the conditions that reduce redeposition include using a halogen-containing composition that is metered to the substrate and gate stack in gaseous form.

33. (Previously Presented) A process of forming a gate stack comprising:

providing a substrate;

forming a gate dielectric layer over the substrate;

depositing a polysilicon layer over the gate dielectric layer;

forming a metal film above the polysilicon layer;

forming a cap layer over metal film;

etching a gate stack through the cap layer, the metal film, and the polysilicon layer, under conditions that reduce redeposition on the substrate of a volatilized portion of the metal film;

wherein at least one process of depositing a polysilicon layer, forming a metal film, and forming a cap layer is carried out in the presence of a metal-reducing composition;

following etching a gate stack, further comprising:

oxidizing the polysilicon layer under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film;

forming a spacer layer over the gate stack under conditions that reduce redeposition on the substrate and the gate stack of a volatilized portion of the metal film; and

wherein the conditions that reduce redeposition include using NF_3 gas that is metered to the substrate and gate stack.

34. (Original) The process according to claim 31, wherein the conditions that reduce redeposition include using a halogen-containing composition disposed in a layer or the film in the gate stack, and a halogen-containing composition that is metered to the substrate and gate stack in gaseous form.

35. (Original) The process according to claim 31, wherein the conditions that reduce redeposition include using fluorine disposed in the cap layer over the metal film.

36-66. (Canceled)